REMARKS

Claim Rejections Under 35 U.S.C. § 112

Claims 1, 6, 16, 19 and 20 were rejected under 35 U.S.C. §112, first paragraph, as "failing to comply with the written description requirement." Applicant respectfully traverses this rejection.

The "dedicated bus" as claimed by Applicant is clearly shown in the drawings and implicitly described in the present specification. Figure 2 shows that the bus between the volatile memory 204 and the non-volatile memory 206 is not coupled to any other device. This bus is thus dedicated to the volatile memory 204 and the non-volatile memory 206.

Claim Rejections Under 35 U.S.C. § 102

Claims 1 and 3-5 were rejected under 35 U.S.C. § 102(e) as being anticipated by *Dye* (U.S. Patent No. 6,145,069). Applicant respectfully traverses this rejection.

The Examiner states that the circuits that are to the left of the data buffer 160 are equivalent to the non-volatile device of the present invention. However, the Examiner is randomly assembling a non-volatile device that is inconsistent with the disclosure of *Dye*.

Dye discloses a flash memory system 900 that includes the compression enhanced flash memory controller 200 of which the data buffer 160 is a part. In other words, everything within reference 900 is part of a non-volatile memory device. This is clearly shown in Figures 3 and the overall system diagram of Figure 4 in which the memory device 900 is shown coupled to a RAM device 440 over a system bus 118. The memory system 900 is described in *Dye* starting at column 8, line 18.

It is also well known by those skilled in the art that a flash memory array 100 is simply comprised of memory cells that require a controller (i.e., CEFMC 200), addressing circuitry (i.e., compression control unit & data directory 300), power (i.e., DC/DC converter 190) and bus interface (i.e., bus I/F 180). The Examiner, by randomly choosing blocks from the flash memory system 900 of Dye would leave a plurality of blocks that could not operate as a memory device. Therefore, *Dye* neither teaches nor suggests Applicant's invention as claimed since the non-volatile device 900 of *Dye* is not connected to a volatile memory device 420 or 440 over a dedicated bus without intervention by another device.

Claim Rejections Under 35 U.S.C. § 103

Claims 2, 5-7, 9 and 10 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Dye* in view of *Harari et al.* (U.S. Patent No. 6,266,724), and further in view of *Fallon et al.* (U.S. Patent Application Publication No. 2002/069354). Claim 19 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* (U. S. Patent No. 6,058,474), in view of Iverson (U. S. Patent No. 6,332,172). Claims 16-18 were rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.* in view of Iverson and further in view of *Harari et al.* Claim 8 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Dye*, *Harari et al.* and *Fallon et al.*, and further in view of *Baltz et al.* Claim 20 was rejected under 35 U.S.C. § 103(a) as being unpatentable over *Baltz et al.*, *Iverson*, and *Harari et al.*, as applied to claim 16, and further in view of *Shin* (U. S. Patent No. 6,735,669). Applicant respectfully traverses this rejection.

Dye is discussed above. Applicant has shown that *Dye* neither teaches nor suggests Applicant's invention as claimed.

Baltz et al., at col. 7, lines 46 – 60, clearly states that "DMA0 100 transfers 1024 32-bit words of data from external 8-bit ROM 671..." Figure 8 also shows a dotted line from the DMA0 100 device to the bus 73 between the internal memory 23 and EPROM 671. This clearly shows and describes not only control but also intervention of the transfer process by the DMA0 device 100 in transferring a predetermined quantity of data words.

Baltz et al. contains numerous other references to such intervention and control by the DMA device. For example, col. 1, lines 53 – 60 states in part that "direct memory access (DMA) circuitry which is operable to transfer data from an external source of data to the internal memory." This passage additionally states that the DMA initialization circuitry causes the DMA circuitry to transfer data.

Control of the data transfer process of *Baltz et al.* is synonymous with intervention. It may be possible to intervene in a process without controlling it (e.g., monitoring or buffering), however Applicant is unclear as to how it is possible to control a process without intervening in that process. Since Applicant's invention as claimed is to a system that decompresses and transfers data to a volatile memory device over a dedicated bus without intervention, *Baltz et al.* neither teaches nor suggests Applicant's invention.

Harari et al. discloses a mother card 10 that includes a controller 41 and functional modules 42. Two of the possible functions of these modules 42 are the compression and decompression of data. *Harari et al.* neither teaches nor suggests Applicant's invention of the

non-volatile memory decompressing and transferring data to the volatile memory over a dedicated bus without intervention.

Fallon et al. discloses methods and systems for accelerated loading of operating systems. None of the systems disclose or suggest a non-volatile memory with a decompression algorithm that transfers decompressed data over a dedicated bus to a volatile memory without intervention, as claimed by Applicant.

Shin discloses a Rambus RAM that has various modes for low power system operation. *Shin* neither teaches nor suggests Applicant's invention as claimed in the amended claims.

Even if it were obvious to combine *Dye*, *Harari et al.*, *Fallon et al.*, *Baltz et al.* and/or *Shin* in any combination, and Applicant maintains that it is not, no combination of the references can teach or suggest Applicant's invention. None of the references teach or suggest Applicant's invention as claimed in the amended claims for storing compressed data from a processor in a non-volatile memory having a decompression capability that decompresses the data as it is being transferred, without intervention, to a volatile memory over a dedicated bus.

CONCLUSION

For the above-cited reasons, Applicant respectfully requests that the Examiner allow the claims of the present application. If the Examiner has any questions or concerns regarding this application, please contact the undersigned at (612) 312-2211. No new matter has been added and no additional fee is required by this response.

Respectfully submitted,

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